What is claimed is:

1. A multichip module comprising:

a circuit section having an insulating layer, a patterned interconnect having connection lands formed on first and second surfaces of said insulating layer and an interlayer via for electrically interlayer connect said connection lands formed said first and second surfaces of said insulating layer;

an electric chip having connection terminals connected to said connection lands, and mounted on said first surface of said insulating layer with said connection terminals connected to said connection lands for processing an electric signal inputted and/or outputted through said interlayer via; and

an optical chip having a terminal section connected through said interlayer via to said connection land with said connection terminal connected thereto, having a light emitting section and/or a photo detecting section formed on a surface thereof and buried in said insulating layer with said surface coinciding with a second surface of said insulating layer so that said light emitting section and/or said photo detecting section is exposed on said second surface of said insulating layer.

2. The multichip module according to Claim 1, wherein:

said circuit section comprises said patterned interconnect formed on a surface of a plurality of said insulating layers which are stacked and said interlayer via interlaying said patterned interconnect;

said electric chip is mounted on an uppermost layer among said stacked plurality of insulating layers; and

said optical chip is buried in a lowermost layer among said stacked plurality of insulating layers.

3. The multichip module according to Claim 1, wherein said optical chip is buried in a direction of thickness of said insulating layer and within a region of projection of said electric chip.

4. A multichip module manufacturing method comprising the steps of:

forming a circuit section having an insulating layer and a patterned interconnect having connection lands formed on first and second surfaces of said insulating layer;

mounting an electric chip having connection terminals connected to said connection lands on a first surface of said insulating layer with said connection terminals connected to said connection lands;

burying an optical chip having a terminal section constituting an electric signal input/output section and a light emitting section and/or a photo detecting section formed on a surface thereof in said insulating layer with said surface coinciding with a second surface of said insulating layer so that said light emitting section and/or said photo detecting section is exposed on said second surface of said insulating layer; and

forming an interlayer via on said circuit section for performing interconnecting said connection lands formed on both surfaces of said insulating layer, and electrically interlayer connecting said connection lands and a terminal section of said optical chip.

5. The multichip module manufacturing method according to Claim 4, wherein:

said circuit section forming step comprises stacking a plurality of said insulating layers and forming said patterned

interconnect on a surface of said plurality of said insulating layers;

said electric chip mounting step comprises mounting said electric chip on an uppermost layer among said stacked plurality of insulating layers; and

said optical chip burying step comprises burying said optical chip in a lowermost layer among said stacked plurality of insulating layers.

6. The multichip module manufacturing method according to Claim 4, wherein said burying step comprises burying said optical chip in a direction of thickness of said insulating layer and within a region of projection of said electric chip.

7. A multichip unit comprising:

a multichip module comprising:

a circuit section having an insulating layer, a patterned interconnect having connection lands formed on first and second surfaces of said insulating layer and an interlayer via for electrically interlayer connect said connection lands formed said first and second surfaces of said insulating layer;

an electric chip having connection terminals connected to said connection lands, and mounted on the a surface of said insulating layer with said connection terminals connected to said connection lands for processing an electric signal inputted and/or outputted through said interlayer via; and

an optical chip having a terminal section connected through said interlayer via to said connection land with said connection terminal connected thereto, having a light emitting section and/or a photo detecting section formed on a surface thereof and buried in said insulating layer with said surface

coinciding with a second surface of said insulating layer so that said light emitting section and/or said photo detecting section is exposed on said second surface of said insulating layer; and

anoptoelectrical interconnect layer comprising:

an optical transmission line formed on a second surface of said insulating layer of said multichip module, for optically connecting said light emitting section and said photo detecting section exposed on said second surface of said insulating layer; and

a via electrically connected with said connection land of said multichip module.

8. The multichip unit according to claim 7, wherein said optical transmission line of saidoptoelectrical interconnect layer comprises an optical wave-guide for making an optical signal generated in said emitting section reflect and propagate to said photo detecting section.

9. The multichip unit according to Claim 7, wherein:

said circuit section of said multichip module comprises said patterned interconnect formed on a surface of a plurality of said insulating layers which are stacked, and said interlayer via interlaying said patterned interconnect;

said electric chip is mounted on an uppermost layer among said stacked plurality of insulating layers; and

said optical chip is buried in a lowermost layer among said stacked plurality of insulating layers.

10. The multichip unit according to Claim 7, wherein said optical chip is buried in a direction of thickness of said insulating layer and within a region of projection of said

electric chip.

11. A multichip unit manufacturing method comprising:

a multichip module forming process comprising the steps of:

forming a circuit section having an insulating layer and a patterned interconnect having connection lands formed on first and second surfaces of said insulating layer;

mounting an electric chip having connection terminals connected to said connection lands on a first surface of said insulating layer with said connection terminals connected to said connection lands;

burying an optical chip having a terminal section constituting an electric signal input/output section and a light emitting section and/or a photo detecting section formed on a surface thereof in said insulating layer with said surface coinciding with a second surface of said insulating layer so that said light emitting section and/or said photo detecting section is exposed on said second surface of said insulating layer; and

forming an interlayer via on said circuit section for performing interconnecting said connection lands formed on both surfaces of said insulating layer, and electrically interlayer connecting said connection lands and a terminal section of said optical chip; and

an optoelectrical interconnect layer forming process comprising the steps of:

forming an optical transmission line on a second surface of said insulating layer of said multichip module, for optically connecting said light emitting section and said photo detecting section exposed on said second surface of said insulating layer; and

forming a via electrically connected with said connection

land of said multichip module.

12. The multichip unit manufacturing method according to claim 11, wherein saidoptoelectrical interconnect layer forming process comprises a step of forming an optical wave-guide as said optical transmission line, for making an optical signal generated in said emitting section reflect and propagate to said photo detecting section.

13. The multichip unit manufacturing method according to Claim 11, wherein:

said circuit section forming step of said multichip module forming process comprises stacking a plurality of said insulating layers and forming said patterned interconnect on a surface of said plurality of said insulating layers;

said electric chip mounting step comprises mounting said electric chip on an uppermost layer among said stacked plurality of insulating layers; and

said optical chip burying step comprises burying said optical chip in a lowermost layer among said stacked plurality of insulating layers.

14. The multichip unit manufacturing method according to Claim 11, wherein said burying step of said multichip module forming process comprises burying said optical chip in a direction of thickness of said insulating layer and within a region of projection of said electric chip.